In the Claims:

Cancel Claims 5 and 11, without prejudice.

B1 C

6. The FET of claim 7, wherein said second implant comprises an extension implant.

7. An FET, comprising:

a gate having a top and bottom portion, the top portion having a width that is greater than the width of the bottom portion;

B2 C

a first diffusion self-aligned to the bottom portion;

a second implant defined by said top portion; and a spacer adjacent said top portion and a third implant defined by said spacer.

B3

10. The FET of claim 20, wherein said first conductive material is on a gate dielectric and said gate dielectric is on a substrate.

B4

12. The FET of claim 20, wherein said first material comprises a first semiconductor material.

B5

15. The FET of claim 20, wherein said second conductive material comprises polysilicon.

16. The FET of claim 20, wherein said first conductive material comprises polysilicon.

19. The FET of claim 20, wherein said second conductive material comprises a silicide.

B6 SUB C1

20. An FET, comprising a gate, said gate comprising first conductive material and a second conductive material different from said first conductive material, said second conductive material on said first conductive material, wherein said second conductive material extends beyond said first conductive material to provide a T-shaped gate, wherein said first material has a dimension less than a photolithographic minimum dimension, and a spacer along sidewalls of said second conductive material.